July 8, 1994
GFK-0761F

IMPORTANT PRODUCT INFORMATION

READ THIS INFORMATION FIRST

Product: **Programmable Controller CPU Module**
IC697CPU731U
IC697CPU732H
IC697CPU771S
IC697CPU772H

This is the production release of the IC697 PLC CPU modules version 5.00. The purpose of this release is to support Sequential Function Chart user programs, Parameterized Subroutines, other new features described in "New Features and Functionality", and to fix the problems listed in "Problems Resolved by This Upgrade". This is also the initial release of the Model 924 CPU module.

Table 1. Catalog Numbers

New Catalog Number	Replaces
IC697CPU731U	IC697CPU731P, RU, R, S, T
IC697CPU732H	IC697CPU732D, EU, E, F, G
IC697CPU771S	IC697CPU771M, NU, N, P, R
IC697CPU772H	IC697CPU772D, EU, E, F, G

Identification

Hardware and software identification is summarized in the following tables.

Table 2. Hardware Identification

Catalog Number	Board Identification	Board Revision
IC697CPU731U	CPFB2	44A731660-G01 R02 or later
IC697CPU732H	CPFB2	44A731660-G01 R02 or later
IC697CPU771S	CPFB2	44A731660-G01 R02 or later
IC697CPU772H	CPFB2	44A731660-G01 R02 or later

Table 3. Software Identification

Catalog Number	EPROM Location	EPROM Label
IC697CPU731U	U67 U66	395-005E5.00 395-006E5.00
IC697CPU732H	U67 U66	395-003F5.00 395-004F5.00
IC697CPU771S	U67 U66	395-007E5.00 395-008E5.00
IC697CPU772H	U67 U66	395-001F5.00 395-002F5.00

Update Information

Release 5 is not compatible with some older versions of the CPU731 and CPU771; specifically, CPU731A through N and CPU771A through L are *not upgradable* to Release 5. You must replace CPU731A through N with IC697CPU731T, and CPU771A through L must be replaced with IC697CPU771R. All other Model 731 and 771, and Models 732 and 772 CPUS can be upgraded with the kits shown in the following table.

Table 4. Upgrade Kits

Upgrade Kit	For Upgrading	To
44A731236-G04	IC697CPU731P, RU, R, S, T	IC697CPU731U
44A731230-G05	IC697CPU732D, EU, E, F, G	IC697CPU732H
44A731237-G04	IC697CPU771M, NU, N, P, R	IC697CPU771S
44A731231-G05	IC697CPU772D, EU, E, F, G	IC697CPU772H

Documentation

The following table lists the applicable documentation for each of the referenced CPUs.

Table 5. User Documentation

Catalog Number	Data Sheet	User Manual
IC697CPU731U	GFK-0159F	see below
IC697CPU732H	GFK-0581A	see below
IC697CPU771S	GFK-0349D	see below
IC697CPU772H	GFK-0588B	see below

Read this document before installing or attempting to use the IC697CPU731, IC697CPU732 , IC697CPU771, or IC697CPU772 PLC CPU Modules. For more information, refer to the applicable *Programmable Controller Installation manual*, *Programming Software User's Manua*l, and *Programmable Controller Reference Manual*.

Special Operation Notes

IC641 Compatibility

1. This release of the PLC CPU modules is compatible with the versions of IC641 programming software listed in the table below. However, version 5.00 or later is required to gain access to all of the CPU's features and functionality. To work around a compatibility problem with serial IC641 programming software, the PLC will return 3.50 as its version to all serial IC641 programming software products (WSI and Standard COM) release 3.04 and earlier.

CPU Model	IC641 Programming Software
731	Version 2.04 or later
732	Version 3.01 or later
771	Version 2.04 or later
772	Version 3.01 or later

If Release 5 PLC CPU firmware is used with IC641 programming software Release 4.01 or 4.02, the PLC Sweep Control and Monitor screen (F3 F8) should **ONLY** be used to change (tune) the constant window or constant sweep time. Any other use may result in the background window time being incorrectly set to 255 milliseconds. For these IC641 programming software releases used with a Release 5 CPU, the configuration package must be used to set the desired sweep modes or window times.

PCM and BTM Compatibility

2. With the introduction of timing improvements and new features in release 5.00, it is highly recommended that systems using PCMs use IC697PCM711J or later. It is also highly recommended that systems using BTMs use IC697BEM713B or later. Use of boards of an earlier revision may result in lower system performance.

Notice to Upgrade GBC Hardware

3. With the introduction of new features in this release, timings with the IC66* Bus Controllers (GBCs / NBCs) have changed; this has uncovered a problem in the GBC / NBC firmware. GBCs / NBCs in expanded racks could be lost if the system is fully configured and only the main rack cycles power.

   It is recommended to update existing GBC/NBC hardware with Bus Controller IC697BEM731K or later when updating PLC CPU firmware to release 5.00.

Foreign VME Modules

4. IC641 programming software Release 5.00 allows foreign VME modules to be configured for five modes: BUS INTERFACE, INTERRUPT ONLY, FULL MAIL, I / O SCAN, and REDUCED MAIL. However, Release 5 and earlier supports only the BUS INTERFACE mode. *The other modes should not be configured.*

Maximum PLC Sweep

5. In systems configured for IC66* Bus Redundancy a complete PLC sweep must be executed every 500 ms or less, even though it is possible to configure the watchdog timer to higher limits. This also means that resetting of the watchdog timer with Service Request #8 cannot be done indefinitely.

Serial Communications

6. The following operational restrictions exist for the Serial Communications feature:

   1. Serial communications may add up to 5 ms of time to any given sweep. This should be taken into account when setting the watchdog timer.

   2. The following procedure is recommended when changing baud rates in the PLC and the WSI board. First enter the configuration package and change the baud rate on the PLC, then store the new configuration. Now power off the PLC and then go to the WSI setup screen and change the WSI baud rate. Finally, power the PLC back on.

   3. The link idle time setting in IC641 programming software Config for Serial Communications should be set to 10 seconds or greater. Otherwise a communications failure will occur when storing the config to the PLC.

Serial Port Mode Configuration

7. There is a serial port configuration parameter under software configuration for the PLC called MODE. This configuration parameter can be one of two values: **SNP** to indicate that the serial port will be used for SNP communications, or **MSG** to indicate that the serial port will be used to send printf commands from a C program block to the connected device. If you have configured MODE to be **MSG** and are also using serial IC641 programming software as a means of communicating with the PLC, communications with IC641 programming software is lost when going to the RUN mode, since the serial port is currently configured for printf commands from C program blocks.

IC641/WSI Attach

8. Do not connect or disconnect the WSI/BTM cable while the programmer host is powered-on. This action may cause a running PLC to Stop.

Expansion Rack ID

9. The expansion racks for the IC641 PLC are shipped with the rack ID strapped for rack 0 (the main rack). If the rack jumper is not changed the PLC will not recognize the rack at all and may not properly identify the error.

Expansion Rack Cable

10. Do not connect or disconnect the expansion rack cable while the CPU is running. This will cause the PLC to go to the STOP/HALT mode.

Expansion Rack Power

11. Expansion racks should be powered up at the same time that the main rack is powered up, or they should be powered up after the main rack has completed its power-up initialization. *Do not power-up an expansion rack while the CPU is running power-up diagnostics.*

Memory Usage

12. A general rule-of-thumb for memory usage is 48 bytes per I/O point plus register memory in bytes.

Timer Operation

13. Care should be taken when timers (ONDTR, TMR, and OFDTR) are used in program blocks that are NOT called every sweep. The timers accumulate time across calls to the sub-block unless they are reset. This

means that they function like timers operating in a program with a much slower sweep than the timers in the main program block. For program blocks that are inactive for large periods of time, the timers should be programmed in such a manner as to account for this catch up feature.

Similar to this are timers that are skipped because of the use of the JUMP instruction. Timers that are skipped will NOT catch up and will therefore not accumulate time in the same manner as if they were executed every sweep..

I/O Link Interface

14. When powering up the PLC CPU without a battery and I/O Link Interface boards are present, an incorrect "Loss of Module" fault will be logged for each I/O Link Interface board; but the PLC CPU will not consider these boards as lost, and the boards will continue to operate properly.

Constant Sweep

15. Constant Sweep time, when used, should be set to about 10 ms greater than the normal sweep time to avoid any oversweep conditions when monitoring or performing on-line changes with the programmer. The smallest valid constant sweep time setting is 10 milliseconds for the Model 781, 782, 914, and 924 PLCs and 18 milliseconds for the other CPUs. Window completion faults will occur if the constant sweep setting is not high enough.

Interaction of IC641 Programming Software with Closed Programming Window

16. The IC641 programming software Sweep Control and Monitor screen cannot be used to change the PLC Sweep Modes or timers (Constant Sweep Time, Program Window Times, etc.) while the program window is closed. Use Service Requests #1 through #4 to perform these functions.

Caution

IC641 programming software cannot be used to change the PLC mode (STOP, RUN, etc.) while the programming window is closed. Use the toggle switch on the CPU module instead.

Problems Resolved by This Upgrade

1. If the CPU's toggle switch is moved to STOP and back to RUN while a C block is sending text out the serial port, the serial port used to stop working and the CPU had to be power cycled to make SNP and C block messages work again. This no longer happens: the serial port should continue to work.
2. When power is cycled on an expansion rack in a system that is running a large sweep time when IC641 programming software is not connected, GBCs / NBCs in that rack will now configure properly.

New features and Functionality

Sequential Function Chart

1. Release 5 of the PLC CPU together with Release 5 of the IC641 programming software has the ability to create, load / store, and execute Sequential Function Chart (SFC) user programs. SFC is a method specifically developed for describing industrial sequential control systems. SFC is a graphic method which represents the functions of a sequential automated system as a sequence of steps and transitions. Each step represents commands or actions that are either active or inactive. The flow of control passes from one step to the next through a conditional transition that is either True (1) or False (0). If the transition condition is true (1), indicated by setting the transition variable, control passes from the active step, which becomes inactive, to the next step, which then becomes active.

Parameterized Subroutine Blocks

2. A Parameterized Subroutine Block (PSB) is an optional user-defined function block, configured with between zero (o) and seven (7) input / output parameter pairs. A parameterized subroutine enables you to reuse relay ladder logic within the same program or in multiple programs. Logic which needs to be repeated can be entered in a parameterized subroutine. Calls would then be made to that subroutine to access the logic. In this way, total program size is reduced. Dividing a program into smaller subroutines simplifies programing and reduces the overall amount of logic needed for the program. Release 5 of the PLC CPU together with Release 5 of the IC641 programming software has the ability to create, load / store, and execute parameterized Subroutine Blocks.

RANGE Function Block

3. A new RANGE function block has been added, which is used to compare a single input value against two delimiters to determine whether the input value falls within the range of delimiters. Release 5 of IC641 programming software is required for this feature.

ARRAY RANGE Function Block

4. A new Array RANGE function block has been added, which is used to compare a single input value against two arrays of delimiters that specify an upper and lower bound to determine whether the input value falls within the range specified by the delimiters. Release 5 of IC641 programming software is required for this feature.

Background Task Window

5. There are now PLC diagnostic tests that will run in the Background Task Window. The background Timer configuration value defaults to zero. If you want the tests to run in the Background Window, then change the Background Timer to a non-zero value. Also, refer to *Additions to the PLC Reference Manual* for a description of SVCREQ #5: Change Background Task Window State and Values.

Restrictions and Open Problems

1. If an expansion rack powers up while the CPU in the main rack is in the RUN mode, the slot fault contacts will prematurely indicate that the modules in the expansion rack are not faulted *before* they complete their power up.
2. In a multi-rack system, false LOSS OF RACK faults may occur when the system loses power. If this fault is configured to be fatal, the system will power-up in STOP mode.
3. When there is no logic stored in a CPU module the %Q and %M tables will be cleared when the CPU is placed in RUN mode. In this context "no logic stored" means that no program had ever been stored or that the clear function on the IC641 programming software had been used to clear logic and configuration.
4. When the Bit Sequencer sequences from one step to another, the negative transitional contact that corresponds to the original step is not set. The transition contact for the new step is set and remains set until the sequencer sequences to the next step. This operation is identical to the operation of the previous versions of the CPU firmware.
5. If multiple faults exist in an IC697 PLC remote drop and one of them is corrected, a FAULT contact that uses the remote drop's module reference will incorrectly indicate that no faults exist at the remote drop.
6. User application faults logged for Service Request #21 can only use error codes between 0 and 2047. Use of any other error codes could cause the PLC to treat the alarms as Remote Scanner alarms.
7. An IC66* Bus Fault may set the fault condition for the M_rsbmm (r=rack, s=slot, b=bus, mm=SBA of GBC / NBC) fault and nofault contacts. This fault condition will persist until either the fault tables are cleared or the GBC's / NBC's rack is power-cycled.
8. An Analog Input Base module and its expander modules may not come online if they are configured in an expansion rack that is missing when the main rack powers up. Power-up the expansion rack first, then power-up the main rack.
9. If the main rack loses power during PLC configuration, analog input base boards (ALG230) in expansion racks that do not lose power may fail. The failure would occur on the subsequent configuration. PLC configuration occurs during power up, store of configuration, and reads from Retentive (Flash) Memory. To prevent the failure, tie all racks to a common power source. To correct the failure, power-cycle the expansion racks.

Additions to the PLC Reference Manual

The following information will be added to a future version of the *Programmable Controller Reference Manual*.

SVCREQ #5: Change Background Task Window State and Values

Use the SVCREQ function with function number 5 in order to enable or disable the background task window. The change will occur in the same CPU sweep in which the function is called.

When the window is enabled, the function returns the current time value for the window. When the window is disabled, it remains disabled until enabled again. The SVCREQ function will always pass power flow to the right for this function number.

For the Change Background Task Window function, the parameter block has a length of 1 word.

To disable the background task window, enter SVCREQ function 5 with this parameter block:

0	0	address

To enable the background task window, enter SVCREQ function #5 with this parameter block:

Mode	Value from 1 to 255 ms	address

Example:

In the following example, when enabling contact FST_SCN is set in the first scan, the MOVE function establishes a default value of 20 ms for the background task window, using a parameter block beginning at %P00050. Later in the program when input %I00500 transitions on, the state of the background task window toggles on and off. The parameter block for all three windows is at location %P00051. Since the time for the background task window is the third value in the parameter block returned from the Read Window Values function (function #2), the location of the existing window time for the system communications window is %P00053.